REMARKS

Claims 1-45 are currently pending in the subject application and are presently under consideration. Applicants' representative notes with appreciation the indication that claims 37 and 38 would be allowable if rewritten in independent form to recite limitations of respective base claims and any intervening claims. It is believed such amendments are not necessary in view of the comments herein. However, applicants' representative reserves the option to recast such claims at a later date if necessary.

Favorable reconsideration of the subject patent application is respectfully requested in view of the comments and amendments herein.

I. Rejection of Claims 1-36 and 39-45 Under 35 U.S.C. § 103(a)

Claims 1-36 and 39-45 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Bourgoin *et al.* (U.S. 5,804,709). This rejection should be withdrawn for at least the following reasons. Bourgoin *et al.* does not teach or suggest all limitations recited in the subject claims.

> To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness. A *prima facie* case of obviousness is established by a showing of three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* MPEP §706.02(j). The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *See In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

The subject application relates to characterization of capacitance and resistance relating to interconnects within VLSI circuits. (*See e.g.*, pg. 1, lns. 6 and 7). In particular, the subject application relates to non-contact in-line characterization of capacitance and resistance of VLSI circuit interconnects. (*See e.g., id.* at lns. 6-10). Characterization refers to measurement of capacitance, resistance, and/or physical parameters related to VLSI circuit interconnects. (*See*

e.g., pg. 2 ln. 29 to pg. 3, ln. 1). Interconnects refers to interconnect lines, which can be metal or poly-silicon that is part of active or passive devices, contacts, vias, ground signal paths, or a combination thereof. (*See e.g.*, pg. 6, lns. 15-17).

Claims 1-28:

Independent claim 1 (from which claims 2-28 depend) recites *a system that facilitates non-invasive in-line characterization of parameters of VLSI circuit interconnects, comprising: **a plurality of micro-electro-mechanical system cantilevers that apply voltage(s) to VLSI circuit interconnect(s) without physical contact thereto**...a measuring component that measures **deflections(s) [that] correspond to electrical forces generated from the applied voltage(s) as passed through VLSI circuit interconnects**...* Bourgoin *et al.* does not teach or suggest such novel features.

Bourgoin *et al.* relates to measuring forces and/or deflections of cantilever type elements in the field of Atomic Force Microscopy. (*See e.g.*, col. 1, lns. 4-7). Bourgoin *et al.* further relates to a method and apparatus for determining material properties and in particular, to a dopant profiler based on a scanning probe microscope involving the generation and detection of higher harmonics of an applied electromagnetic field. (*See e.g.*, col. 1, lns. 7-12).

In the Final Office Action, it is asserted that Figures 2 through 4 of Bourgoin *et al.* disclose the subject claims. However, these figures simply disclose basic variants wherein a flexible cantilever 220 with a tip at its apex and a sample holder 230 with an associated sample 231 are connected to a DC voltage source 250, which provides a bias voltage across the interface. (*See e.g.*, col. 7, lns. 27-31). The cantilever and its associated tip may oscillate at its resonance frequency or at a frequency of an externally supplied signal. (*See e.g., id.* at 31-34). A gap separating the cantilever tip and the sample is modulated causing the emission of radiation that includes fundamental microwave signal ω and higher harmonic frequencies $n\omega$ signals that are subsequently received by an antenna and amplified for further processing. (*See e.g., id.* at lns. 34-39).

Assuming *arguendo* that the sample 231 of Fig 2A is the VLSI circuit interconnect(s), as contended by the Examiner, the cantilever 220 is not applying voltage(s) to the VLSI circuit interconnect(s) (or sample 231), as claimed. Bourgoin *et al.* clearly discloses that the cantilever 220 and the sample holder 230 with a sample 231 are connected to the DC voltage source 250.

(*See e.g.*, col. 7, lns. 27-31). Thus, it is not the cantilever 220 applying the voltage to the sample 231, but the DC voltage source 250 or the sample holder 230 that would be applying the voltage. Additionally, since Bourgoin *et al.* does not disclose that the cantilever(s) are applying voltage(s) to the VLSI circuit interconnect(s), it cannot teach or even suggest deflection(s) corresponding to electrical forces generated from the applied voltage(s) *as passed through VLSI circuit interconnect(s)*, as claimed.

As conceded in the Final Office Action, Bourgoin *et al.* only discloses one MEMS cantilever. Therefore, it is contended in the Final Office Action that it "would have been obvious to one having ordinary skill in the art at the time the invention was made to provide additional MEMS since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art, *St. Regis Paper Co. v. Bemis Co.* 193 USPQ 8." (*See e.g.*, Final Office Action page 3). However, the novel features of the subject claims are not "mere duplication of the essential working parts of a device." Figures 9-17 of the subject application illustrate exemplary systems that facilitate in-line characterization of VLSI circuit interconnects without requiring contact. A series of AC voltages are applied to a pair of cantilevers to effectuate characterization of the VLSI circuit interconnects. (*See e.g.*, pgs. 20, lns. 9-10). These characteristics include measurement of coupling capacitance *between* interconnects, capacitance between an interconnect and a substrate (acting as a ground), and measurement of parasitic capacitance. (*See e.g., id.* at lns. 10-13). This is clearly distinct from Bourgoin *et al.* that discloses simply measuring a fundamental microwave signal ω and higher harmonic frequencies $n\omega$.

Accordingly, based on at least the foregoing, a *prima facie* case of obvious has not been established. There is no teaching, suggestion or motivation to modify Bourgoin *et al.* absent utilizing applicants' specification as a 20/20 hindsight based roadmap to provide the necessary motivation. The rationale proffered to modify the reference is to achieve benefits identified in applicants' specification rather than the cited reference. Applicants' representative respectfully submits that this is an unacceptable and improper basis for a rejection under 35 U.S.C. §103. (*See Interconnect Planning Corporation v. Thomas E. Feil, Robert O. Carpenter, V Band Systems, Inc., and Turret Equipment Corp.*, 774 F.2d 1132, 1138 (Fed. Cir. 1985) (stating the invention must be viewed not with the blueprint drawn by the inventor, but in the state of the art that existed at the time of the invention)). In essence, this rejection is based on an assertion that

it would have been obvious to do something not suggested in the art because so doing would provide advantages stated in applicants' specification. This sort of rationale has been condemned by the Court of Appeals for the Federal Circuit. (*See Panduit Corp. v. Dennison Manufacturing Co.*, 1 USPQ2d 1593 (Fed. Cir. 1987)). Therefore, it is requested that this rejection be withdrawn and the subject claims allowed.

Claims 29-31:

Independent claim 29 (from which claims 30 and 31 depend) recites *a system that facilitates characterization of VLSI circuit interconnects, comprising: a voltage source that outputs a plurality of disparate voltages,* ***two or more micro-electro-mechanical system cantilevers that receive the voltage ....and apply the voltage(s) to VLSI circuit interconnects(s), wherein a first MEMS cantilever contacts a first VLSI interconnect and a second MEMS cantilever does not physically contact a VLSI interconnect*** ... Bourgoin *et al.* does not teach or suggest such novel features.

As discussed *supra* with regard to claims 1-28, Bourgoin *et al.* does not teach or suggest cantilever(s) that apply voltage(s) to the VLSI circuit interconnect(s). In addition, as conceded, Bourgoin *et al.* discloses only one cantilever, and, therefore, cannot teach or suggest a first cantilever that contacts a first VLSI interconnect and a second cantilever that does not physically contact a VLSI interconnect. Providing one of the cantilevers in contact with one interconnect can facilitate a more expedient characterization of the interconnects. (*See e.g.*, pg. 11, lns. 18-20). This is more than mere duplication of parts as contended in the Final Office Action and requires more than routine skill in the art.

According, based on at least the foregoing, this rejection should be withdrawn.

Claims 32-45:

Independent claim 32 (from which claims 33-42 depend) recites *a method that facilitates measurement of various parameters of VLSI circuit interconnects, comprising: positioning* ***at least two MEMS cantilevers with conductive tips*** *in proximity to at least two adjacent VLSI circuit interconnects, providing voltage(s) to the conductive tips;* ***injecting current(s) into the VLSI circuit interconnects via the conductive tips***... Independent claim 43 (from which claims

44 and 45 depend) recites similar limitations. Bourgoin *et al.* does not teach or suggest such novel features.

As discussed above, it has been conceded by the Examiner that Bourgoin *et al.* only discloses one cantilever. However, the subject claims recite novel aspects that go beyond mere duplication of essential parts and would not be obvious to one having ordinary skill in the art. In addition, as discussed *supra*, Bourgoin *et al.* also fails to disclose injecting current(s) into the VLSI circuit interconnects *via* the conductive tips of at least two MEMS cantilevers. In fact, Bourgoin *et al.* is silent regarding these novel features.

Based on at least the foregoing, this rejection should be withdrawn and the subject claims allowed.

CONCLUSION

The present application is believed to be in condition for allowance in view of the above comments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [SIPRP101US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

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